INFORMATION DISCLOSURE CITATION PTO-1449	Customer Number 26615	ATTORNEY'S DKT NO. H1491	APPLICATION NO. ~~Unassigned~~ 10/653,234
		APPLICANT(S) Bin Yu et al.	
		FILING DATE September 3, 2003	GROUP ~~Unassigned~~ 2818

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes	Translation No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

dhn	Digh Hisamoto et al.: "FinFET - A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325.
dhn	Yang-Kyu Choi et al.: "Sub-20nm CMOS Fin FET Technologies," 2001 IEEE, IEDM, pages 421-424.
dhn	Xuejue Huang et al.: "Sub-50 nm P-Channel Fin FET," IEEE Transactions on Electron Devices, Vol. 48, No..5, May 2001, pages 880-886.
dhn	Yang-Kyu Choi et al.: "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pages 25-27.
dhn	Xuejue Huang et al.: "Sub 50-nm FinFET: PMOS," 1999 IEEE, IEDM, pages 67-70.
dhn	Co-pending U.S. Patent Application Serial No. 10/632,965, filed August 4, 2003, entitled: "Semiconductor Device Having A Thin Fin And Raised Source/Drain Areas," Haihong Wang et al.; 18 page specification and 19 sheets of drawings.

EXAMINER	DATE CONSIDERED
	03/22/05

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).